What is claimed:

1. An integrated circuit comprising:

a substrate including one or more devices;

a first insulating layer overlying the substrate having one or more first level vias connecting to the one or more devices in the substrate; and

a second insulating layer overlying the first insulating layer, the second insulating layer including one or more conductive structures formed above and connecting to the one or more first level vias, each of the one or more conductive structures including:

a first level metal line;

a barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms formed on the number of first level vias; and

a seed layer having a thickness in the range of 5 to 150 Angstroms formed at least between a portion of the barrier/adhesion layer and the first level metal line.

2. The integrated circuit of claim 1, wherein the second insulating layer includes a foamed polymer layer.

3. The integrated circuit of claim 1, wherein the second insulating layer includes a foamed polyimide layer.

4. The integrated circuit of claim 2, wherein first insulating layer includes a Si_3N_4 layer having a thickness between about 100 Angstroms to about 500 Angstroms.

5. The integrated circuit of claim 1, wherein the barrier/adhesion layer includes one or more of titanium, zirconium, and hafnium.

6. The integrated circuit of claim 1, wherein the seed layer includes copper and the first level metal line includes a copper metal line.

7. The integrated circuit of claim 1, wherein the integrated circuit is a memory device.

8. An integrated circuit comprising:

a substrate including one or more devices;

an insulator layer overlying the substrate, the insulator layer having one or more first level vias connecting to the one or more devices in the substrate; and

a polymer layer overlying the insulator layer, the polyimide layer including one or more conductive structures formed above and connecting to the one or more first level vias, each of the one or more conductive structures including:

a first level metal line;

a barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms formed on the number of first level vias; and

a seed layer having a thickness in the range of 5 to 150 Angstroms formed at least between a portion of the barrier/adhesion layer and the first level metal line.

9. The integrated circuit of claim 8, wherein the polymer layer includes a polyimide layer.

10. The integrated circuit of claim 8, wherein the insulator layer includes Si_3N_4 having a thickness between about 100 Angstroms to about 500 Angstroms.

11. The integrated circuit of claim 8, wherein the barrier/adhesion layer includes one or more of titanium, zirconium, and hafnium.

12. The integrated circuit of claim 8, wherein the seed layer includes copper.

13. The integrated circuit of claim 8, wherein the integrated circuit is a memory device.

14. An integrated circuit comprising:

a substrate including one or more devices;

an insulator layer overlying the substrate having one or more first level vias connecting to the one or more transistors in the substrate; and

an oxide layer overlying the insulator layer including one or more conductive structures formed above and connecting to the one or more first level vias, each of the one or more conductive structures including:

a layer of titanium or zirconium having a thickness of approximately 50 Angstroms disposed on a first level via of the number of first level vias;

a first layer of aluminum on the layer of titanium or zirconium having a thickness of approximately 50 Angstroms;

a layer of copper on the first layer of aluminum having a thickness of approximately 10 Angstroms; and

a second layer of aluminum on the layer of copper having a thickness of approximately 50 Angstroms.

15. The integrated circuit of claim 14, wherein the insulator layer includes Si3N4 having a thickness between about 100 Angstroms to about 500 Angstroms.

16. The integrated circuit of claim 14, wherein the oxide layer includes a fluorinated silicon oxide layer.

17. The integrated circuit of claim 14, wherein the integrated circuit is a memory device.

18. An integrated circuit comprising:

a number of first level vias in a first insulator layer connecting to a number of silicon devices in a substrate; and

a first number of conductive structures formed over and connecting to the number of first level vias in the first insulator layer, each conductive structure, each conductive structure of the first number of conductive structures including:

a layer of zirconium having a thickness of approximately 15 Angstroms disposed on a first level via of the number of first level vias;

a seed layer of copper on the layer of zirconium having a thickness of approximately 50 Angstroms; and

a copper metal line formed on the seed layer of copper; and

a polymer layer surrounding the first number of conductive structures.

19. The integrated circuit of claim 18, wherein each conductive structure further includes a layer of aluminum having a thickness of approximately 50 Angstroms formed between the seed layer of copper and the copper metal line.

20. The integrated circuit of claim 18, wherein the polymer layer includes a foamed polymer layer.

21. The integrated circuit of claim 18, wherein the integrated circuit further includes:

a second number of conductive structures including a number of second level vias and a number of second level metal lines formed above and connecting to the first number of conductive structures, wherein each of the second number of conductive structures includes:

a layer of zirconium having a thickness of approximately 15 Angstroms;

a seed layer of copper on at least a portion of the layer of zirconium having a thickness of approximately 50 Angstroms; and

a core copper conductor over the seed layer and within the layer of zirconium.

22. The integrated circuit of claim 18, wherein the integrated circuit is a memory device.

23. An integrated circuit comprising:

a number of first level vias in a first insulator layer connecting to a number of silicon devices in a substrate;

a first number of conductive structures formed over and connecting to the number of first level vias in the first insulator layer, each conductive structure, comprising:

a first barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms disposed on a first level via of the number of first level vias;

a first seed layer formed on at least a portion of the barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms; and

a first core conductor formed on the first seed layer;

a polymer surrounding the first number of conductive structures; and

a second number of conductive structures include a number of second level vias and a number of second level metal lines, wherein the second number of conductive structures are formed over and connect to the first number of conductive structures, and wherein each of the second number of conductive structures includes:

a second barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms;

a second seed layer formed on at least a portion of the barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms; and

a second core conductor formed on the second seed layer.

24. The integrated circuit of claim 23, wherein the second number of conductors is surrounded by a polyimide layer.

25. The integrated circuit of claim 24, wherein the polyimide layer includes a foamed polyimide layer.

26. The integrated circuit of claim 23, wherein the first and the second barrier/adhesion layers include one or more of tantalum nitride, titanium, zirconium, and hafnium.

27. The integrated circuit of claim 23, wherein the first and the second core conductors include a metal conductor having one or more of aluminum, copper, silver, and gold.

28. The integrated circuit of claim 23, wherein the first and the second seed layers include one or more of aluminum, copper, silver, and gold.

29. The integrated circuit of claim 18, wherein the integrated circuit is a memory device.

30. An integrated circuit comprising:

a number of first level vias in a first insulator layer connecting to a number of transistors in a substrate; and

an oxide layer formed over the number of first level vias in the first insulator layer, wherein the oxide layer includes a number of conductive structures connecting from a top surface of the oxide layer to the number of first level vias, each conductive structure comprising:

a layer of tantalum nitride having a thickness of approximately 5 to 100 Angstroms disposed on a first level via of the number of first level vias;

a seed layer of copper on the layer of tantalum nitride having a thickness of approximately 100 Angstroms; and

a copper metal line formed on the seed layer of copper.

31. The integrated circuit of claim 30, wherein each conductive structure further includes a layer of tantalum nitride forming a top surface of each conductive structure such that the top surface of each conductive structure is level with the top surface of the oxide layer.

32. The integrated circuit of claim 30, wherein the oxide layer includes a fluorinated silicon oxide layer.

33. The integrated circuit of claim 30, wherein at least one of the number of first level vias is filled with tungsten.

34. The integrated circuit of claim 30, wherein at least one of the number of first level vias is within a titanium silicide liner.

35. The integrated circuit of claim 30, wherein the integrated circuit is a memory device.

36. An integrated circuit comprising:

a first level via in a first insulator layer connecting to a transistor in a substrate; and

an oxide layer formed over the first level via in the first insulator layer, wherein the oxide layer includes a conductive structure connecting from a top surface of the oxide layer to the first level via, the conductive structure including:

a barrier/adhesion layer having two material layers, the barrier/adhesion layer disposed on a first level via of the number of first level vias;

a seed layer on the barrier/adhesion layer;

a layer of aluminum on the seed layer, the layer of aluminum having a thickness of about 50 Angstroms; and

a metal line formed on the layer of aluminum.

37. The integrated circuit of claim 36, wherein the barrier/adhesion layer has a thickness of approximately 5 to 100 Angstroms.

38. The integrated circuit of claim 36, wherein the barrier/adhesion layer includes one or more of titanium, zirconium, and hafnium.

39. The integrated circuit of claim 36, wherein the seed layer includes one or more of silver and gold.

40. The integrated circuit of claim 36, wherein the first level via is a tungsten via and is contained in a liner.

41. The integrated circuit of claim 36, wherein the first level via is contained in a liner that separates the first level via from a layer of Si_3N_4.

42. The integrated circuit of claim 36, wherein the seed layer has a thickness of approximately 10 Angstroms.

43. The integrated circuit of claim 36, wherein the integrated circuit is a memory device.

44. An integrated circuit comprising:

a first level via in a first insulator layer connecting to a transistor in a substrate;

a titanium silicide liner that contains the first level via;

a conductive structure formed over the first level via in the first insulator layer, the conductive structure including:

a barrier/adhesion layer disposed on the first level via;

a seed layer on the barrier/adhesion layer; and

a metal line disposed above the seed layer; and

a second insulator layer containing the conductive structure.

45. The integrated circuit of claim 44, wherein the barrier/adhesion layer has a thickness in the range of 5 to 150 Angstroms.

46. The integrated circuit of claim 44, wherein the barrier/adhesion layer includes CuTi.

47. The integrated circuit of claim 44, further including a layer of aluminum between the seed layer and the metal line.

48. The integrated circuit of claim 44, wherein the second insulator layer includes a fluorinated silicon oxide layer.

49. The integrated circuit of claim 44, wherein the integrated circuit is a memory device.

50. An integrated circuit comprising:

a first level via in a first insulator layer connecting to a transistor in a substrate;

a first conductive structure formed over the first level via in the first insulator layer, the first conductive structure including:

a first barrier/adhesion layer disposed on the first level via;

a first seed layer disposed on the first barrier/adhesion layer; and

a first metal line disposed above the first seed layer;

a second insulator layer containing the first conductive structure;

a second conductive structure having a portion disposed on the first metal line of the first conductive structure, the second conductive structure including:

a second barrier/adhesion layer disposed on the first metal line;

a second seed layer disposed on the second barrier/adhesion layer; and

a second metal line disposed above the second seed layer.

51. The integrated circuit of claim 50, further including a layer of aluminum between the first seed layer and the first metal line.

52. The integrated circuit of claim 50, further including a layer of aluminum between the second seed layer and the second metal line.

53. The integrated circuit of claim 50, wherein the first metal line and the second metal line are composed of different materials.

54. The integrated circuit of claim 50, wherein the first metal line and the second metal line each include one or more of copper, aluminum, silver, and gold.

55. The integrated circuit of claim 50, wherein the first and the second seed layers include one or more of aluminum, copper, silver, and gold.

56. The integrated circuit of claim 50, wherein the first and the second barrier/adhesion layers each have a thickness in the range of 5 to 150 Angstroms.

57. The integrated circuit of claim 50, wherein the first and second barrier/adhesion layers each include one or more of titanium, zirconium, and hafnium.

58. The integrated circuit of claim 50, wherein the integrated circuit is a memory device.

59. An integrated circuit, comprising:

a first level via in a first insulator layer connecting to a silicon device in a substrate;

a liner containing the first level via;

a first conductive structure formed over the first level via in the first insulator layer, the first conductive structure including:

a first barrier/adhesion layer disposed on the first level via;

a first seed layer disposed on the first barrier/adhesion layer; and

a first metal line disposed above the first seed layer;

a second insulator layer containing the first conductive structure;

a second conductive structure having a portion disposed on the first metal line of the first conductive structure, the second conductive structure including:

a second barrier/adhesion layer disposed on the first metal line;

a second seed layer disposed on the second barrier/adhesion layer; and

a second metal line disposed above the second seed layer.

60. The integrated circuit of claim 59, wherein the liner contains titanium silicide.

61. The integrated circuit of claim 59, wherein the liner separates the via from a layer of Si_3N_4.

62. The integrated circuit of claim 59, wherein the first metal line and the second metal line each include one or more of copper, aluminum, silver, and gold.

63. The integrated circuit of claim 59, wherein the first and second barrier/adhesion layers each have a thickness in the range of 5 to 150 Angstroms.

64. The integrated circuit of claim 59, wherein the first and second barrier/adhesion layers each include one or more of titanium, zirconium, and hafnium.

65. The integrated circuit of claim 59, wherein the integrated circuit is a memory device.

66. A system, comprising:

a processor; and

an integrated circuit coupled to the processor, wherein the integrated circuit includes:

a substrate including one or more devices;

a first insulating layer overlying the substrate having one or more first level vias connecting to the one or more devices in the substrate; and

a second insulating layer overlying the first insulating layer, the second insulating layer including one or more conductive structures formed above and connecting to the one or more first level vias, each of the one or more conductive structures including:

a first level metal line;

a barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms formed on the number of first level vias; and

a seed layer having a thickness in the range of 5 to 150 Angstroms formed at least between a portion of the barrier/adhesion layer and the first level metal line.

67. The system of claim 66, wherein the second insulating layer includes a polymer layer.

68. The system of claim 66, wherein the second insulating layer includes a foamed polymer layer.

69. The system of claim 66, wherein the barrier/adhesion layer includes one or more of titanium, zirconium, and hafnium.

70. The system of claim 66, wherein the seed layer includes copper and the first level metal line includes a copper metal line.

71. The system of claim 66, wherein the integrated circuit is a memory device.

72. A system, comprising:

a processor; and

an integrated circuit coupled to the processor, wherein the integrated circuit includes:

a substrate including one or more transistors;

an insulator layer overlying the substrate having one or more first level vias connecting to the one or more transistors in the substrate; and

a polyimide layer overlying the insulator layer including one or more conductive structures formed above and connecting to the one or more first level vias, each of the one or more conductive structures including:

a first level metal line;

a barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms formed on the number of first level vias; and

a seed layer having a thickness in the range of 5 to 150 Angstroms formed at least between a portion of the barrier/adhesion layer and the first level metal line.

73. The system of claim 72, wherein the barrier/adhesion layer includes one or more of titanium, zirconium, and hafnium.

74. The system of claim 72, wherein the seed layer includes copper and the first level metal lines includes a copper metal line.

75. The system of claim 72, wherein the integrated circuit is a memory device.

76. A system, comprising:

a processor; and

an integrated circuit coupled to the processor, wherein the integrated circuit includes:

a substrate including one or more transistors;

an insulator layer overlying the substrate having one or more first level vias connecting to the one or more transistors in the substrate; and

an oxide layer overlying the insulator layer including one or more conductive structures formed above and connecting to the one or more first level vias, each of the one or more conductive structures including:

a first level metal line;

a barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms formed on the number of first level vias; and

a seed layer having a thickness in the range of 5 to 150 Angstroms formed at least between a portion of the barrier/adhesion layer and the first level metal line.

77. The system of claim 76, wherein the barrier/adhesion layer includes one or more of titanium, zirconium, and hafnium.

78. The system of claim 76, wherein the seed layer includes copper and the first level metal lines includes a copper metal line.

79. The system of claim 76, wherein the integrated circuit is a memory device.